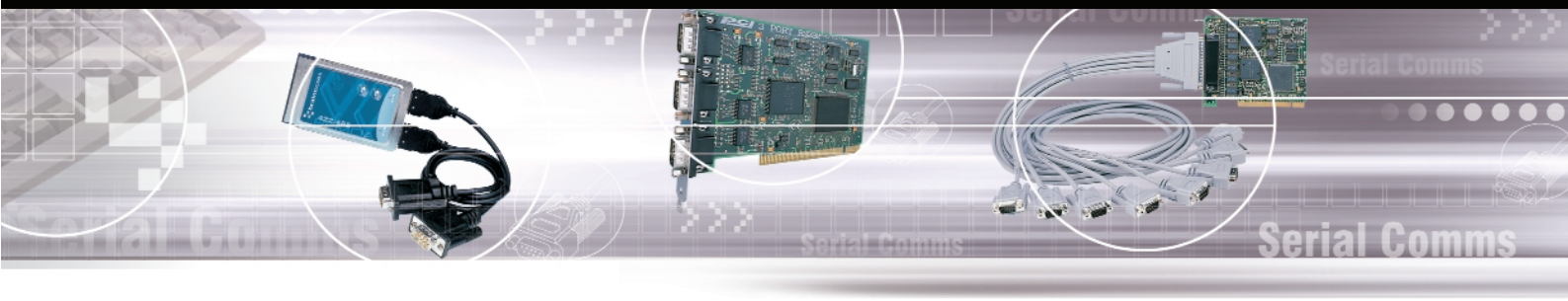


BB16PCI958 Chip

Key Features

- Glueless interface to PCI bus
- Up to eight UARTs
- UARTs are register and functionally compatible with TL16C550 or TL16C750
- Compatible with existing 16C750/550/450 device drivers
- PCI 2.1, 2.2, 2.3 and 3.0 compliant
- Supports both 5.0V and 3.3V PCI signalling
- Low-power design
- Configuration data is held in a small, cheap serial EEPROM
- UART enhancements:
- Clock prescaler allows more baud rate options
- Readable FIFO levels and tuneable trigger levels improve device driver performance
- Programmable "synchronisation factor" allows baud rates up to fclock/4
- Extensions to standard register set are implemented in a safe, easy-to-use way

There are four configurations for the local-side I/O pins:

- Eight RS232 ports
- Four RS232 ports and four RS422/485 ports
- Four RS232 ports and one LPT port
- Four RS232 ports and an ISA-style local-bus interface

The UART-to-port mapping is switchable so that one can configure UARTs 0-3 to all be RS422/485 ports, or port 0 to be RS232 and port 1 RS485.

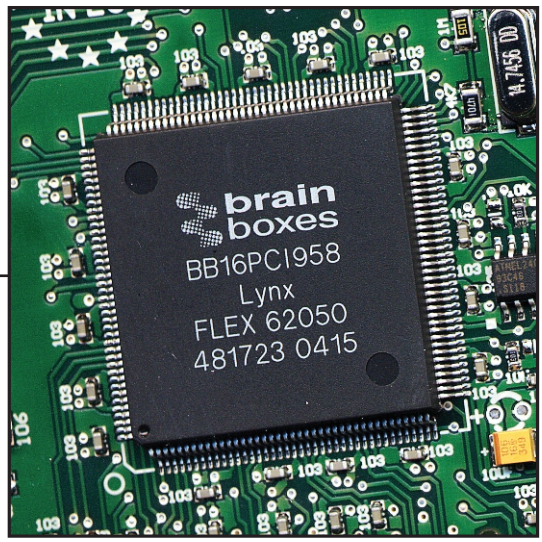
The UARTs can be configured with three different FIFO depth options:

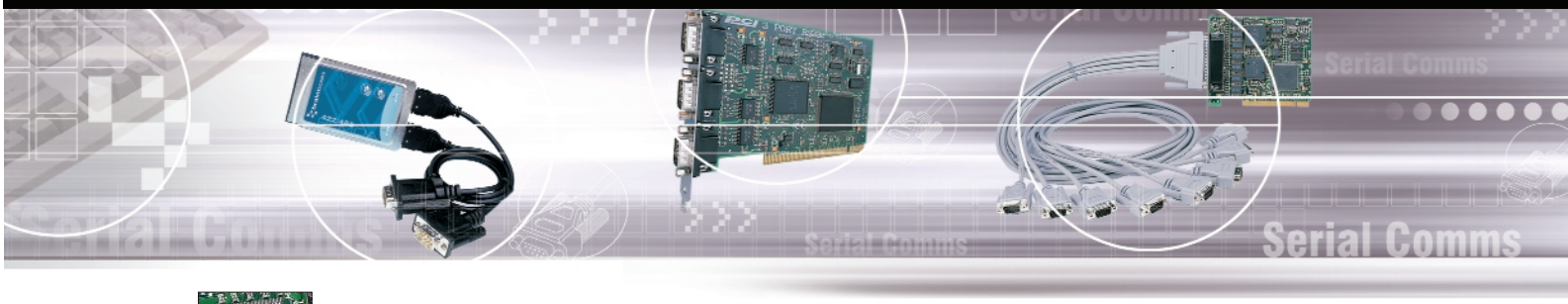
- FIFO depth=32: all eight UARTs usable
- FIFO depth=64: four UARTs (0 to 3) usable
- FIFO depth=128: two UARTs (0 and 1) usable

The UARTs are always TL16C550 compatible, and are also TL16C750 compatible if the FIFO depth is set to a value = 64. Use of FIFO depths other than 1, 16 or 64 requires a BB16PCI958-aware device driver.

General

The BB16PCI958 contains eight UARTs (Universal Asynchronous Receiver-Transmitters) with a host interface suitable for direct connection to a PCI bus. Once installed and configured by the host OS, it provides an eight-byte programming interface which may be configured to be identical to that of the TL16C550A UART from Texas Instruments. It can be configured to fit the requirements of RS232 or RS422/485 applications.





BB16PCI958 Chip

UARTs

The UARTs in the BB16PCI958 are register and functionally compatible with the TL16C750 or TL16C550A. The TL16C750 is a backwards-compatible upgrade of the TL16C550A. The TL16C550A is a backwards-compatible upgrade of the TL16C450. The TL16C550A is a widely supported industry-standard UART with 16-deep transmit and receive FIFOs. Device drivers written specially for the BB16PCI958 can make use of added features such as deeper FIFOs, readable FIFO levels, and individually programmable FIFO trigger levels.

The UARTs convert between RS232-format serial data on separate transmit and receive lines, and byte-wide I/O writes and reads on the host interface. Malformed incoming serial data is flagged along with the data in the receive FIFO. The state of the UART can be found at any time by reading status registers, and modem control (handshaking output) lines can be individually controlled.

Although polled-mode operation is possible, the UART will usually be operated on a host-interrupt basis. The interrupt system is designed to allow efficient handling of interrupt service requests from the UART, for example by using the prioritised interrupt identification register, readable FIFO levels, and tunable FIFO trigger levels.

The internal transmitter and receiver logic runs at a programmable synchronisation factor of 4x, 8x, or 16x the serial baud rate. This internal clock is generated by dividing a reference clock by and integer divisor from 1 to (216 - 1). In this way the UART can accommodate a serial rate of up to 5 500 000 baud (using a 22 MHz input clock).

The LPT Port

The LPT port implementation in the BB16PCI958 is register and functionally compatible with that in the TL16C552. This is an 'SPP' port with bidirectional data transfer capability, also known as a "PS/2 type" port. A buffer-direction output is provided so that external buffers may be used for this port if desired.

The Host Interface

The BB16PCI958 provides a host interface that can be directly connected to a PCI bus. It responds to configuration accesses, and once configured it also responds to I/O and memory accesses for control of the UART. The data for configuration space is read from a small external serial EEPROM at start-up, together with information on how the BB16PCI958 should be set up.

The Package

The package is a standard 160-pin QFP package (JEDEC ref MS-022), with 0.65 mm lead pitch, and a 4.1 mm max height from PCB.